Remarks:

Reconsideration of the application is requested.

Claims 1 and 3-8 remain in the application. Claim 1 has been amended.

In item 2 on pages 3-6 of the above-mentioned Office action, claims 1 and 3-6 have been rejected as being unpatentable over Sun et al. (US Pat. No. 5,612,249) in view of Ahmad (US Pat. No. 6,037,639) under 35 U.S.C. § 103(a). In item 3 on page 6 of the above-mentioned Office action, claims 7-8 have been rejected as being unpatentable over Sun et al. and Ahmad in view of Krautschneider (US Pat. No. 5,854,500) under 35 U.S.C. § 103(a).

The rejection has been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 13, lines 22-25 of the specification and Fig. 4 of the drawings.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

a silicon oxide passivation layer disposed on said side wall of said gate; and

an insulating silicon nitride spacer disposed on said silicon oxide passivation layer, said spacer acting as an oxidation barrier.

The passivation layer (5') is shown in Fig. 4 of the instant application. This added feature corresponds to a passivation step in the method claim 9 allowed in the parent application.

Sun et al. disclose a method for producing a transistor as shown in Fig. 19 thereof. Therein, the left part shows a transistor formed on a semiconductor substrate. A gate oxide 5 is formed on top of conducting regions 24 and a polysilicon gate 6 is disposed between the conducting regions and on top of the gate oxide 5. Silicon oxide spacers 23 are formed on the side walls of the gate.

However, no silicon oxide passivation layer is formed on the side walls of the gate in the transistor according to Sun et al. If the Examiner would consider the oxide spacers 23 as a passivation layer, then no silicon nitride spacers are disposed on the oxide passivaiton layer.

Clearly, Sun et al. do not show a passivation layer or a silicon nitride spacer disposed on the passivaiton layer, as recited in claim 1 of the instant application.

Furthermore, Sun et al. also do not contain any hint toward the provision of a silicon oxide passivation layer disposed on the side walls of the gate and a silicon nitride spacer disposed on the passivation layer.

Ahmad discloses a method for producing a transistor. As shown in Figs. 3 and 4, a polysilicon gate 112 is formed on top of a gate oxide 108. The side walls of the gate are disposed adjacent conductive regions 118. A spacer 126 is formed on the side walls of the gate by oxidation of the gate. A silicon oxide spacer 136 is formed thereon (see column 5, lines 18-19).

Clearly, Ahmad also fails to disclose a silicon oxide passivation layer on which a silicon nitride spacer is formed. In contrast, Ahmad describes in column, lines 41-42 that "the spacer growth may comprise a nitridation step", which would lead a person skilled in the art in a direction opposite to that of the invention of the instant application.

The invention of the instant application provides a (relatively thin) silicon oxide passivation layer on the side wall of the gate and a (relatively thick) silicon nitride spacer on the passivation layer, whereas Ahmad teaches providing a silicon nitride layer on the side wall of the gate and a silicon oxide spacer the silicon nitride layer.

Accordingly, Sun et al. and Ahmad only teach the use of a silicon oxide spacer, not a silicon nitride spacer. However, as already discussed on pages 8 and 9 of the Amendment filed on August 29, 2002 in response to the previous Office action, a silicon nitride spacer has an advantage over a silicon oxide spacer in that self-aligned contacts can be formed when using silicon nitride spacers, whereas great care must be taken in etching when using silicon oxide spacers.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1 and 3-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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February 12, 2003

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Applic. No.: 09/885,553

Marked-Up Version of the Amended Claims:

Claim 1(Twice amended). A MOS transistor in a single-transistor memory cell, comprising:

a semiconductor substrate having a substrate surface, a first conductive region and a second conductive region;

a gate oxide disposed on said substrate surface;

a gate disposed on said gate oxide over an area between said first conductive region and said second conductive region and having at least one side wall adjacent at least one of said conductive regions; [and]

a silicon oxide passivation layer disposed on said side wall of said gate; and

an insulating silicon nitride spacer disposed on said [side wall of said gate] silicon oxide passivation layer, said spacer acting as an oxidation barrier;

said gate oxide insulating said gate from said semiconductor substrate and having a thickened area in a region below said side wall of said gate.